

77.76MHZ, LVCMOS/LVTTL OSCILLATOR REPLACEMENT

ICS840I-77

GENERAL DESCRIPTION

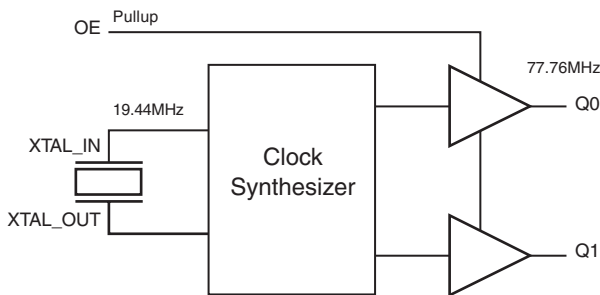


The ICS840I-77 is a SONET Oscillator Replacement and a member of the HiPerClocks™ family of high performance devices from IDT. The ICS840I-77 uses a 19.44MHz crystal to synthesize 77.76MHz. The ICS840I-77 has excellent jitter performance. The ICS840I-77 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

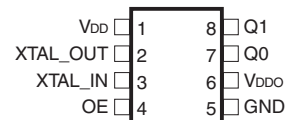
FEATURES

- One LVCMOS/LVTTL output, 15Ω output impedance
- Crystal oscillator interface designed for 19.44MHz, 18pF parallel resonant crystal
- Output frequency: 77.76MHz
- Random jitter: 3ps (typical)
- Deterministic jitter: 0.1ps (typical)
- 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840I-77

8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm package body

G Package

Top View

ICS840I-77

8-Lead SOIC

3.90mm x 4.92mm x 1.37mm body package

M Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V _{DD}	Power		Power supply pin.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	OE	Input	Pullup	Output enable pin. When HIGH, outputs are enabled. When LOW, forces outputs to HiZ state. LVCMOS/LVTTL interface levels.
5	GND	Power		Power supply ground.
6	V _{DDO}	Power		Output supply pin.
7, 8	Q0, Q1	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels. 15Ω output impedance.

NOTE: Pullup refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{OUT}	Output Impedance			15		Ω

TABLE 3. CONTROL FUNCTION TABLE

Control Inputs	Output
OE	Q0, Q1
0	Hi-Z
1	Active

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5 V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	
8 Lead TSSOP	101.7°C/W (0 mps)
8 Lead SOIC	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.0	3.3	3.6	V
V_{DDO}	Output Supply Voltage		3.0	3.3	3.6	V
I_{DD}	Power Supply Current	OE = V_{DD} (output enabled)			80	mA
I_{DDO}	Output Supply Current				20	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.6V$			5	μA
I_{IL}	Input Low Current	$V_{DD} = 3.6V, V_{IN} = 0V$	-150			μA
V_{OH}	Output High Voltage; NOTE 1		2.6			V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

NOTE 1: Outputs terminated with 50 Ω to $V_{DDO}/2$. See Parameter Measurement Information Section, "3.3V Output Load Test Circuit".

TABLE 5. CRYSTAL CHARACTERISTICS

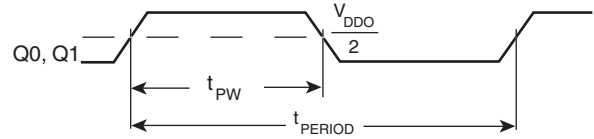
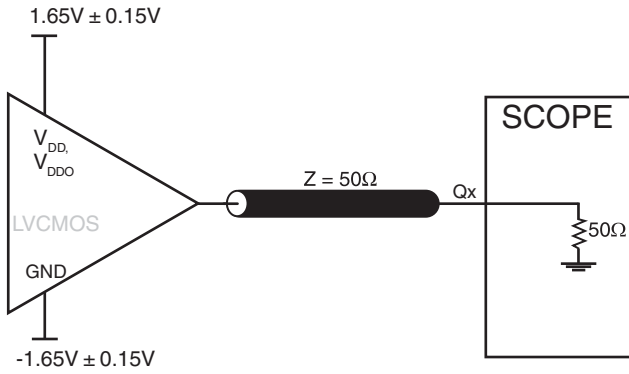
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			19.44		MHz
Equivalent Series Resistance (ESR)				40	Ω
Shunt Capacitance				7	pF
Drive Level				300	μW

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 0.3V$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			77.76		MHz
t_{DJ}	Deterministic Jitter; NOTE 1			0.1		ps
t_{RJ}	Random Jitter; NOTE 1			3		ps
t_{RMS}	RMS of Total Distribution (σ); NOTE 1			3		ps
t_{P-P}	Peak-to-Peak Jitter; NOTE 1			26		ps
t_{OSC}	Oscillation Start Up Time	Time at minimum operating voltage to be 0 s			10	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	400		850	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Measured using Wavecrest SIA-3000.

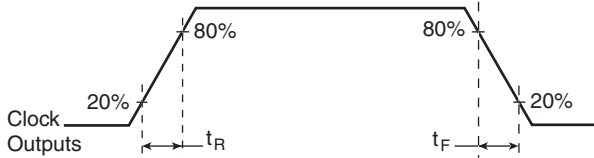
PARAMETER MEASUREMENT INFORMATION



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

3.3V OUTPUT LOAD AC TEST CIRCUIT

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED OUTPUT PINS

OUTPUTS:

LVCMOS OUTPUT:

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

CRYSTAL INPUT INTERFACE

The ICS8401-77 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 19.44MHz, 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

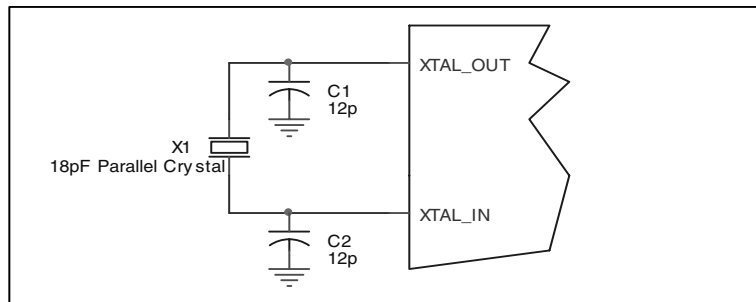


FIGURE 1. CRYSTAL INPUT INTERFACE

RELIABILITY INFORMATION

TABLE 7A. θ_{JA} vs. AIR FLOW TABLE FOR 8 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

TABLE 7B. θ_{JA} vs. AIR FLOW TABLE 8 LEAD SOIC

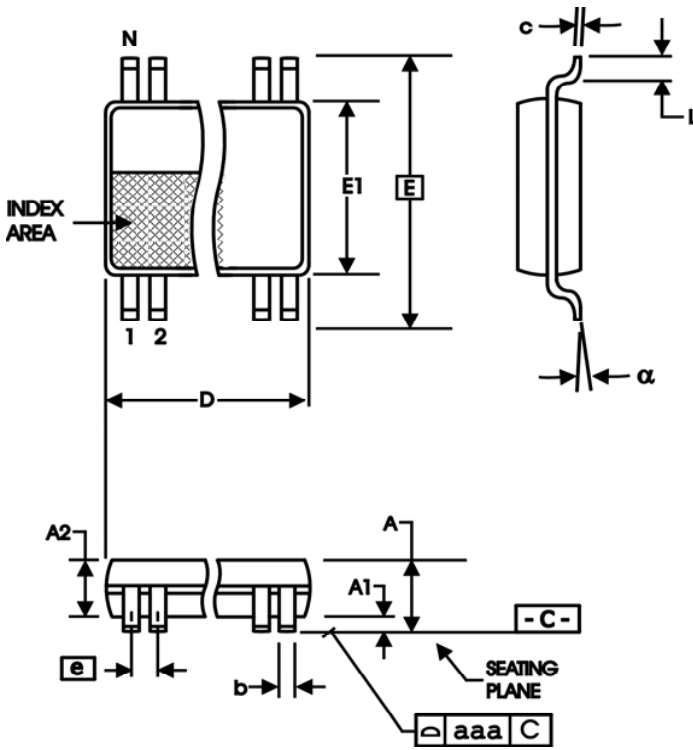
θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS840I-77 is: 2423

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP



PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

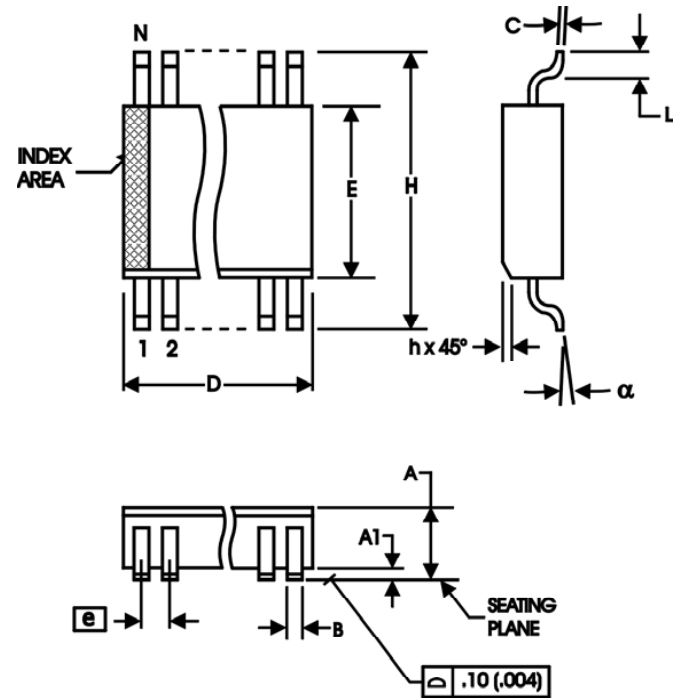


TABLE 8A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS840AGI-77	0AI77	8 lead TSSOP	tube	-40°C to 85°C
ICS840AGI-77T	0AI77	8 lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS840AGI-77LF	TBD	8 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS840AGI-77LFT	TBD	8 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C
ICS840AMI-77	840AMI77	8 lead SOIC	tube	-40°C to 85°C
ICS840AMI-77T	840AMI77	8 lead SOIC	2500 tape & reel	-40°C to 85°C
ICS840AMI-77LF	TBD	8 lead "Lead-Free" SOIC	tube	-40°C to 85°C
ICS840AMI-77LFT	TBD	8 lead "Lead-Free" SOIC	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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